REMARKS

The Office Action mailed April 21, 2003 has been received and reviewed. Claims 1 through 9 and 12 through 19 are currently pending in the application. Claims 1 through 9 and 12 through 19 stand rejected. Applicant has amended claims 1 and 13, and respectfully request reconsideration of the application as amended herein.

This amendment is in response to the Office Action of April 21, 2003.

Claim Objections

Claims 1 and 13 are objected to for informalities within the claims. Applicant has amended claims 1 and 13 to recite "the processor" as opposed to "the host", as requested by the Examiner. Appropriate correction has been made.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So.

Claims 1-3, 5-7, 10 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.** *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-3, 5-7, 10 and 12 are improper because the elements for a *prima facie* case of obviousness are not met to establish a prima facie

case of obviousness regarding the presently claimed invention. Specifically, the rejection of the presently claimed invention fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure, to establish a prima facie case of obviousness.

Claim 1

Regarding amended independent claim 1, Applicants claim:

> A method for compressing video data in a computer system comprising:
> **receiving a current video frame at a core logic chip** in the computer system **from a video source originating the video frame**, the computer system including **the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus**;
> computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the core logic chip, the difference frame including **computing the difference frame in the core logic chip** within the computer system, wherein the core logic chip is a north bridge chip;
> storing the difference frame in the system memory in the computer system; and
> the processor retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data. (Emphasis added.)

Regarding claim 1, Dea and So do not appear to teach or suggest "**receiving a current video frame at a core logic chip . . . from a video source originating the video frame** . . . **the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus**; **computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip** . . . the difference frame including **computing the difference frame in the core logic chip** . . .; **storing the difference frame in the system memory** . . .; and the **host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data**", as claimed by Applicants.

Generally, Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there. Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicant, by "receiving a current video frame at a core logic chip . . . from a video source originating the video frame . . . the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" and "computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip . . . the difference frame including computing the difference frame in the core logic chip . . .".

Regarding So, while So gratuitously states that:

> In an architecture where no video is carried on the PCI bus, a VSP used as a graphic accelerator is still important because it is then advantageously provided either at the North Bridge or AGP graphics/video chip location so that advantageous MIPS are provided without substantially loading the PCI bus. (col. 17, lines 24-29)

So, like Dea, does not disclose receiving a current video frame at a core logic chip . . . from a video source originating the video frame . . . the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip . . .wherein computing the difference frame includes computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . .; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data", as claimed by Applicants.

Applicants submit that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference under 35 U.S.C. § 103 would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants'

disclosure. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper. Specifically, any combination of the difference frame generating architecture of Dea, which is exclusively bus interface and memory dependent, as substituted in place of the VSP and North bridge combination of So, would inevitably result in a memory and bus interface combination since the VSP of So is a digital signal processor-core which pulls data, for example frame data, from a memory store over a bus interface.

Applicants submit that since both references are drawn to bus interface and memory store specific disclosures, there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure. Therefore, Applicants respectfully request that the rejection to claim 1, be withdrawn.

Claims 2-3, 5-7 and 12

Regarding claims 2-3, 5-7 and 12, while the Office Action cites further rejections, claims 2-3, 5-7 and 12 depend from amended independent claim 1 which is allowable in view of the preceding remarks. Therefore, for at least their dependency upon allowable claim 1, 2-3, 5-7 and 12 are allowable over the cited prior art and the respective rejections should be withdrawn.

Claims 4, 9, 13 through 17 and 19

Claims 4, 9, 13 through 17 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) and So (U.S. Patent No. 5,909,559), and further in view of Abramatic et al. (U.S. Patent No. 4,546,383).

The 35 U.S.C. § 103(a) obviousness rejections of claims 4, 9, 13-17, and 19 are improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding amended independent claim 13, Applicants claim:

A method for compressing video data in a computer system comprising:
receiving a current video frame at a core logic chip in the computer system **from a video source originating the video frame**, the computer system including **the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus**;
computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the core logic chip, the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes **computing the difference frame in the core logic chip** within the computer system, wherein the core logic chip is a north bridge chip;
storing the difference frame in the system memory in the computer system;
storing the current video frame in the system memory in the computer system;
the processor retrieving the difference frame directly from the system memory; and
compressing the video data using the difference frame to produce compressed video data.
(Emphasis added.)

Dea, So, and Abramatic do not appear to teach or suggest "**receiving a current video frame at a core logic chip . . . from a video source originating the video frame . . . the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip** . . . the difference frame including **computing the difference frame in the core logic chip** . . .; **storing the difference frame in the system memory** . . .; and the **host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data**", as claimed by Applicants.

Generally, Dea teaches or suggests a compression/decompression accelerator 120 which includes a frame difference block 220 for calculating a difference frame from current frame memory 204 and previous frame memory 206 wherein "[a]ll RAM within accelerator 120 must read and write by way of accelerator bus interface 200."(Col. 5, lines 40-42). Such an architecture is clearly visible with reference to FIGS. 1 and 2 where the frame difference block 220 is only accessible by way of bus interface 200 which retrieves the values from the current frame memory 204 and the previous frame memory 206 which where previously stored there.

Therefore, the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicant, by "receiving a current video frame at a core logic chip . . . from a video source originating the video frame . . . the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" and "computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip . . . the difference frame including computing the difference frame in the core logic chip . . .".

Regarding So, while So gratuitously states that:

> In an architecture where no video is carried on the PCI bus, a VSP used as a graphic accelerator is still important because it is then advantageously provided either at the North Bridge or AGP graphics/video chip location so that advantageous MIPS are provided without substantially loading the PCI bus. (col. 17, lines 24-29)

So, like Dea, does not teach or suggest receiving a current video frame at a core logic chip . . . from a video source originating the video frame . . . the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame . . . as the current video frame streams into the core logic chip . . . the difference frame including computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . .; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data", as claimed by Applicants.

Applicants submit that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference under 35 U.S.C. § 103 would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants' disclosure. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper.

Applicants submit that since both references are drawn to bus interface and memory store specific disclosures, there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure.

Regarding Abramatic, the Office Action cites Abramatic alleging that "Abramatic et al. teaches that a form of image compression consists [in] detecting variations (difference) between one image and the next as describe at column 2, lines 53-56 [and that] Abramatic discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image a the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame." (See Office Action, p. 8.) While Abramatic may disclose calculating a difference frame through the use of an exclusive-OR function, neither Dea, So, nor Abramatic, either individually or in any proper combination, teach suggest or motivate each of the elements of Applicants' claim 13 as amended.

Applicants submit that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference and further in view of the Abramatic reference under 35 U.S.C. § 103 would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants' disclosure. Such a rejection is neither within the ambit nor the purview of 35 U.S.C. § 103 and, clearly, improper. Specifically, any combination of the difference frame generating architecture of Dea, which is exclusively bus interface and memory dependent, as substituted in place of the VSP and North bridge combination of So, would inevitably result in a memory and bus interface combination since the VSP of So is a digital signal processor-core which pulls data, for example frame data, from a memory store over a bus interface.

Applicants submit that there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure. Therefore, Applicants respectfully request that the rejection to claim 13, be withdrawn.

Claims 14 through 17 depend from amended independent claim 13 and, for at least that reason, are allowable and the corresponding rejections should be withdrawn.

Claim 8

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent

No. 5,469,208) and So (U.S. Patent No. 5,909,559) as applied to claim 1 above, and further in view of Hardiman (U.S. Patent No. 5,926,223).

The 35 U.S.C. § 103(a) obviousness rejection of claim 8 is improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding claim 8, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claim in claim 8, including all of the claim limitations of the base claim, namely, "computing the difference frame in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 8, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 8 be withdrawn.

Claim 18

Claim 18 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208), So (U.S. Patent No. 5,909,559) and Abramatic et al. (U.S. Patent No. 4,546,383) as applied to claim 13 above, and further in view of Hardiman (U.S. Patent No. 5,926,223).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met regarding the presently claimed invention. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations and the teaching or suggestion to make the claimed

combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

Regarding claim 18, Dea, So, Abramatic, and Hardiman, either individually, or in any combination, do not teach, suggest, or motive Applicants' invention as claim in claim 18, including all of the claim limitations of the base claim, namely, "computing the difference from in the core logic chip . . .; storing the difference frame in the system memory . . ; storing the current video frame in the system memory . . .; the host retrieving the difference frame directly from the system memory; and compressing the video data using the difference frame to produce compressed video data". In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 18, and further in view of the claim taken as a whole and the novelty associated therewith, Applicants respectfully request that the rejection to claim 18 be withdrawn.

ENTRY OF AMENDMENTS

The amendments to claims 1-3, 6, 13, 14, 16, and 19 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1-9 and 12-19 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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